

GENERAL DESCRIPTION

CM6900G is resonant controller tailor for series topology with synchronous operation to achieve high efficiency to meet today's power need. It is used for DC-DC conversion in the offline application. Light load regulation is accomplished by transitioning the controller from frequency modulation mode into PWM mode.

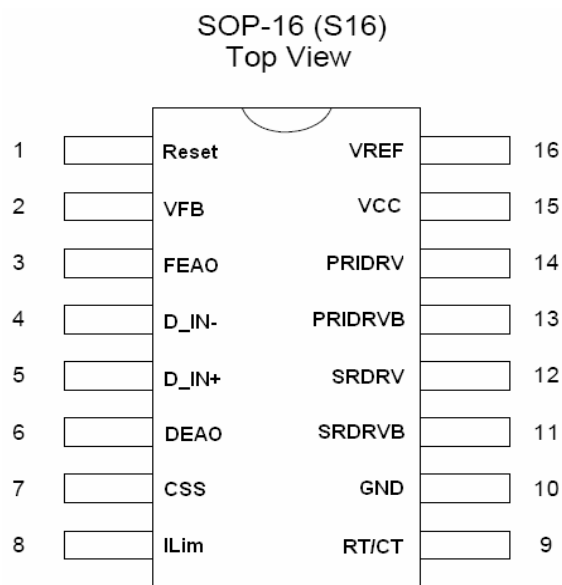
FEATURES

- Supply Voltage Range : 10V to 15V.
- Typical Peak Drive from 12V supply : (PMOS~200 ohm and NMOS~100 ohm).
- UVLO=13V with 3V Hysteresis.
- Reference OK Comparator.
- FM/PWM Mode Operation.
- Softstart Capability with Shutdown Function.
- Latch or Auto-Restart during Current Limit or OVP.

APPLICATIONS

- DC-DC Power Supply.
- LED Lighting Power Supply
- Server Power
- Industrial Power Supply
- High Power Adaptor

CM6900G Pin Configuration

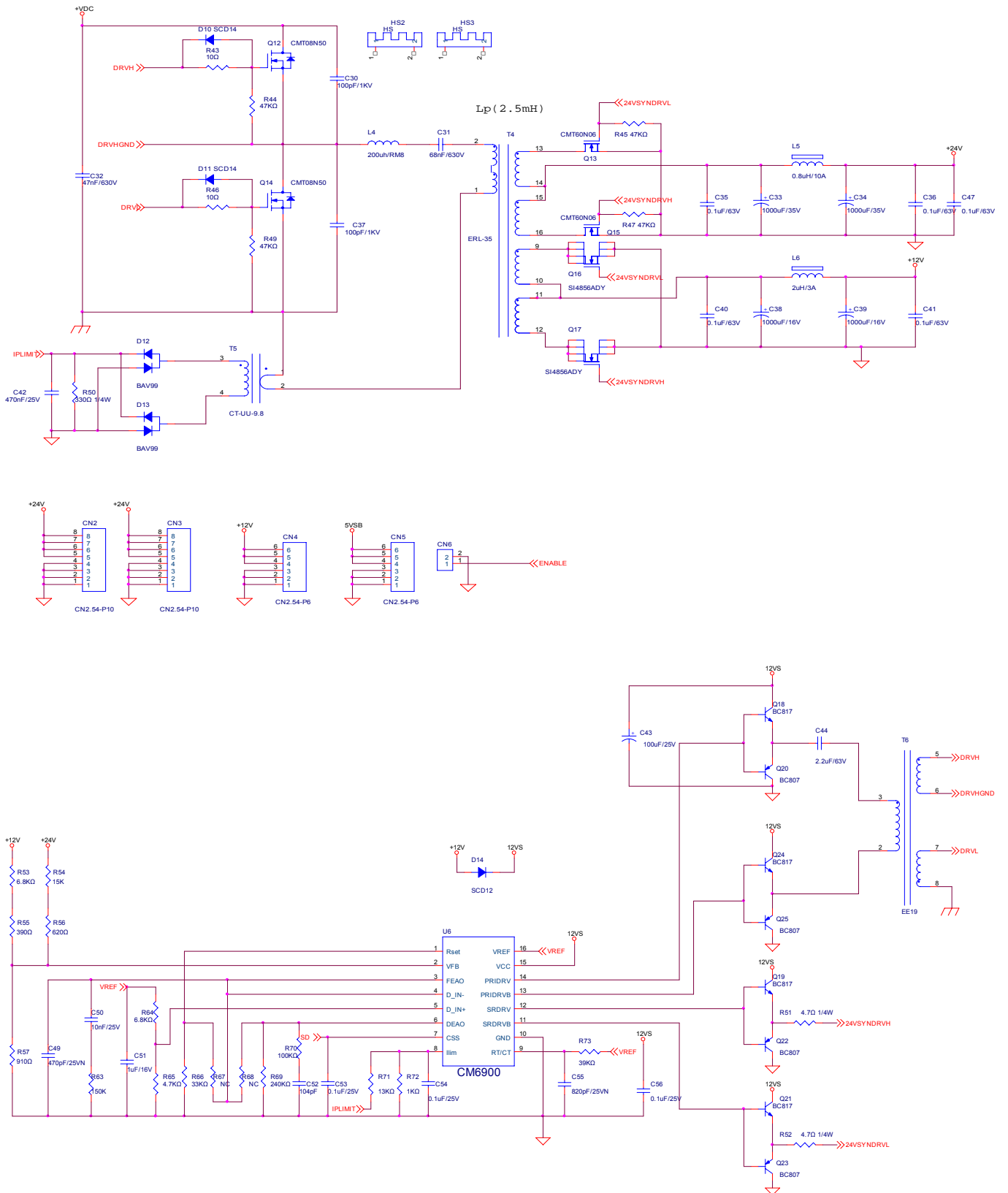


ORDERING INFORMATION

Part Number	Temperature Range	Package
CM6900GIS	-40°C to 125°C	16-Pin SOIC (S016)

*Note: G : Suffix for Pb Free Product

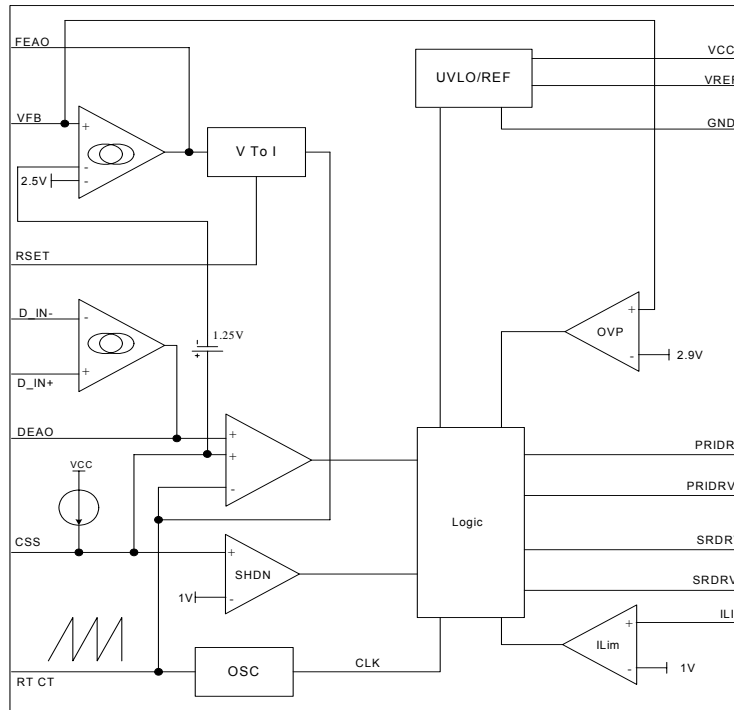
TYPICAL APPLICATION CIRCUIT



PIN DESCRIPTION

Pin No.	Symbol	Description	Operating Voltage			
			Min.	Typ.	Max.	Unit
1	RSET	External resistor which convert FEAO voltage signal into current signal for frequency modulation.	0		5.5	V
2	VFB	Non-inverting input into resonant error amplifier and OVP input.	0	2.5	3	V
3	FEAO	Resonant error amplifier output and compensation node for frequency modulation control.	0		5.5	V
4	D_IN-	Inverting input into PWM error amplifier.	0		6	V
5	D_IN+	Non-inverting input into PWM error amplifier.	0		6	V
6	DEAO	PWM error amplifier output and compensation node for PWM control.	0		4.5	V
7	CSS	Soft start for FM/PWM operation with 1V enable threshold. Also, use for auto-restart operation during current limit.	0		5.5	V
8	ILIM	Input to current comparator with 1V threshold.	0	1	1.25	V
9	RTCT	Oscillator timing components which set the minimum frequency.	1.2		3	V
10	GND	Ground				
11	SDRVB	Synchronous MOSFET driver output.	-0.3		VCC	V
12	SDRV	Synchronous MOSFET driver output.	-0.3		VCC	V
13	PRIDRV	Primary side MOSFET driver output.	-0.3		VCC	V
14	PRIDRVB	Primary side MOSFET driver output.	-0.3		VCC	V
15	VCC	Positive supply for the IC	10	15	17.5	V
16	VREF	Buffered output for the 7.5V voltage reference		7.5		V

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (TA=25°C, unless otherwise specified.)

The following ratings designate persistent limits beyond which damage to the device may occur.

Symbol	Parameter	Value	Unit
VCC	DC Supply Voltage	-0.3 to 20	V
SRDRV	SRDRV Voltage	-0.3 to VCC+0.3	V
SRDRVb	SRDRVb Voltage	-0.3 to VCC+0.3	V
PRIDRV	PRIDRV Voltage	-0.3 to VCC+0.3	V
PRIDRVb	PRIDRVb Voltage	-0.3 to VCC+0.3	V
VREF	VREF Voltage	-0.3 to 7.5	V
RTCT	RTCT Voltage	-0.3 to VREF+0.3	V
VILIM	VILIM Voltage	-0.3 to VREF+0.3	V
CSS	CSS Voltage	-0.3 to VREF+0.3	V
DEAO	PWM Error Amplifier Output Voltage	-0.3 to VREF+0.3	V
D_IN+	Non-Inverting Input Into PWM Error Amplifier Voltage	-0.3 to VREF+0.3	V
FEAO	Resonant Error Amplifier Output Voltage	-0.3 to VREF+0.3	V
VFB	Non-Inverting Input Into Resonant Error Amplifier Voltage	-0.3 to VREF+0.3	V
RSET	V to I Voltage	-0.3 to VREF+0.3	V

ELECTRICAL CHARACTERISTICS

(Vcc=12V, RTCT Freq. =100 KHz, Duty Cycle=50% , Temp=25 degree C, unless otherwise specified.)

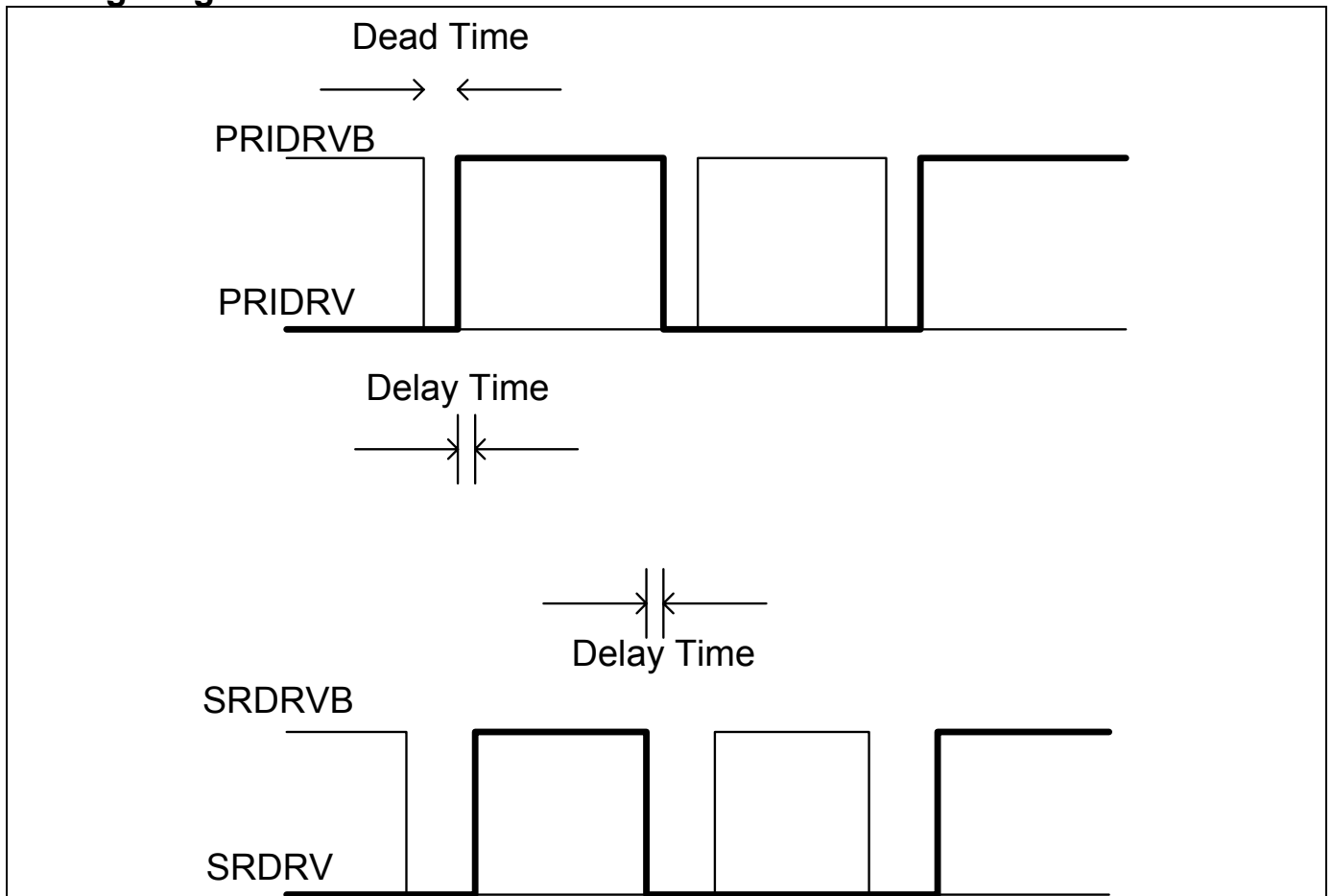
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
VREF (pin 16)						
Reference Voltage	VREF	TA=25°C; Iref=1mA	7.4	7.5	7.6	V
Line Regulation		11V < Vcc < 16.5V		10	25	mV
Load Regulation		0mA < Iref < 7.5mA		10	25	mV
VCC (pin 15)						
VCC Start up voltage	Vstart		12.5	13	13.5	V
UVLO Hysteresics	Hyst			3	3.5	V
Operating Current	ICC			1		mA
PRIDRV,PRIDRVB,SRDRV,SRDRV B (pin 11,12,13 and 14)						
Output Low Voltage	Vol	Isrcrv=-6mA		0.6	1.2	V
Output High Voltage	Voh	Isrcrv=+6mA	9.6	10.8		V
Iout peak source current	Iout			0.12		A
Iout peak sink current	Iout			0.12		A
PMOS Rdson	Rout			200.0	250.0	Ohm
NMOS Rdson	Rout			100.0	150.0	Ohm
Dead Time between PRIDRV and PRIDRVB	TDead			400		ns
Rising Edge Delay Between PRIDRV and SRDRV	Tdelay			500		ns
Falling Edge Delay Between SRDRV and PRIDRV	Tdelay			500		ns
Duty Cycle Range			0		50	%
ILIM (pin 8)						
Threshold Voltage	Vth		0.9	1	1.1	V
CSS (pin 7)						
Soft Start Current	Iss			7.5		uA
Enable Voltage	Ven		0.9	1.0	1.1	V
Enable Hysteresis	Vhyst			75		mV
Auto-restart Upper Threshold	Vup		4.85	5.0	5.15	V
Auto-restart Lower Threshold	Vlw			1-Vhyst		V

ELECTRICAL CHARACTERISTICS

(Vcc=12V, RTCT Freq. =100 KHz, Duty Cycle=50% , Temp=25 degree C, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
FEAO Resonant Error Amplifier (pin 3)						
Input Voltage Range					6	V
Transconductance	Gm			135		umho
Feedback Reference Voltage			2.45	2.5	2.55	V
Input Bias Current			-1	-0.5		uA
Output High Voltage				5.5+VBE		V
Output Low Voltage				0.1	0.4	V
Sink Current				-15		uA
Source Current				15		uA
Open Loop Gain				60		dB
DEAO PWM Error Amplifier (pin 6)						
Input Voltage Range					6	V
Transconductance	Gm			135		umho
Input Bias Current			-1.0	-0.5		uA
Output Voltage High				3+VBE		V
Output Voltage Low				0.1	0.4	V
Sink Current				-15		uA
Source Current				15		uA
Open Loop Gain				60		dB
RTCT Oscillator;RT=61K;CT=470pF (pin 8)						
Initial Accuracy		TA=25'C	95	100	105	Khz
Volatge Stability		11V < Vcc < 16.5V		1		%
Temperature Stability				2		%
Ramp Valley to Peak Voltage				2		V
CT Discharge Time				350		nS
Maxmum Duty cycle		DEAO > 3.0V		50		%
Minimum Duty Cycle		DEAO < 1.2V		0		%
VFB OVP Comparator						
Threshold Voltage				2.94		V
VCC OVP Comparator						
Input Voltage Range				17.5		V

Timing Diagram



Oscillator

The oscillator frequency is determined by the values of RT and CT.

$$f_{osc} = 1 / (t_{RAMP} + t_{DEADTIME})$$

$$t_{RAMP} = RT * CT * \ln((V_{REF} + I_{CHG} * RT - 1.25) / (V_{REF} + I_{CHG} * RT - 3)) \text{ where } I_{CHG} = 4 * (FEAO - V_{BE}) / R_{SET}$$

$$t_{DEADTIME} = 2.125V / 2.5mA * CT = 850 * CT$$

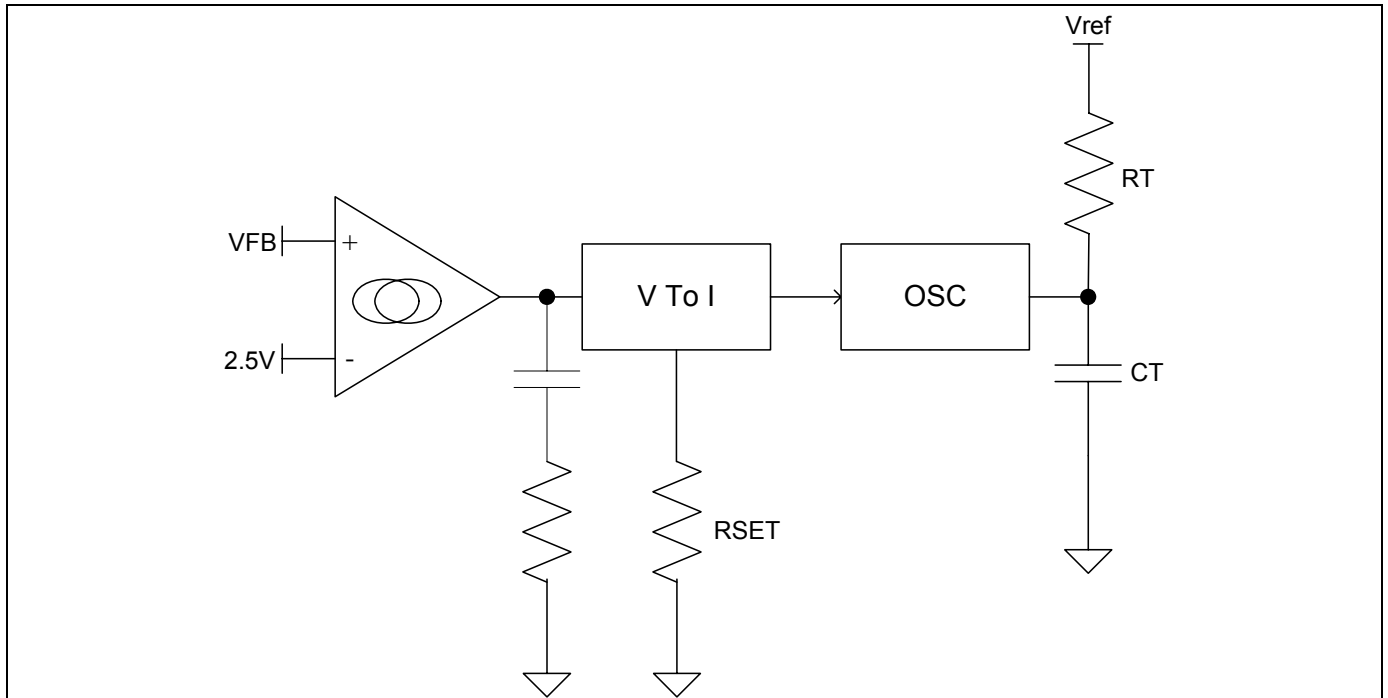
Resonant Section

FM Modulator

Frequency modulation of the resonant controller section is accomplished by controlling the charging current of the oscillator through resonant error amplifier. The frequency of the resonant section is $\frac{1}{2}$ of the oscillator frequency. Compensation is accomplished by connecting R and C in series to the FEAO pin.

$$I_{CHG} = 4 * (FEAO - V_{BE}) / R_{SET}$$

$$I_{CHG(max)} = 20V / R_{SET}$$



PWM Section

Pulse Width Modulator

PWM control is used in voltage mode. In Application 1, when FEAO is equal to the external reference voltage at D_IN+ due to light load, the frequency of the oscillator is fixed at a value determined by the voltage at FEAO, and the controller enters into PWM mode. In this mode, both frequency modulator and pulse width modulator are active.

In Application 2, the offset voltage Vos is externally generated between the VFB pin and D_IN- through a resistor network Rf1, Rf2 and Rf3 in order to separate the interaction between FM mode and PWM mode.

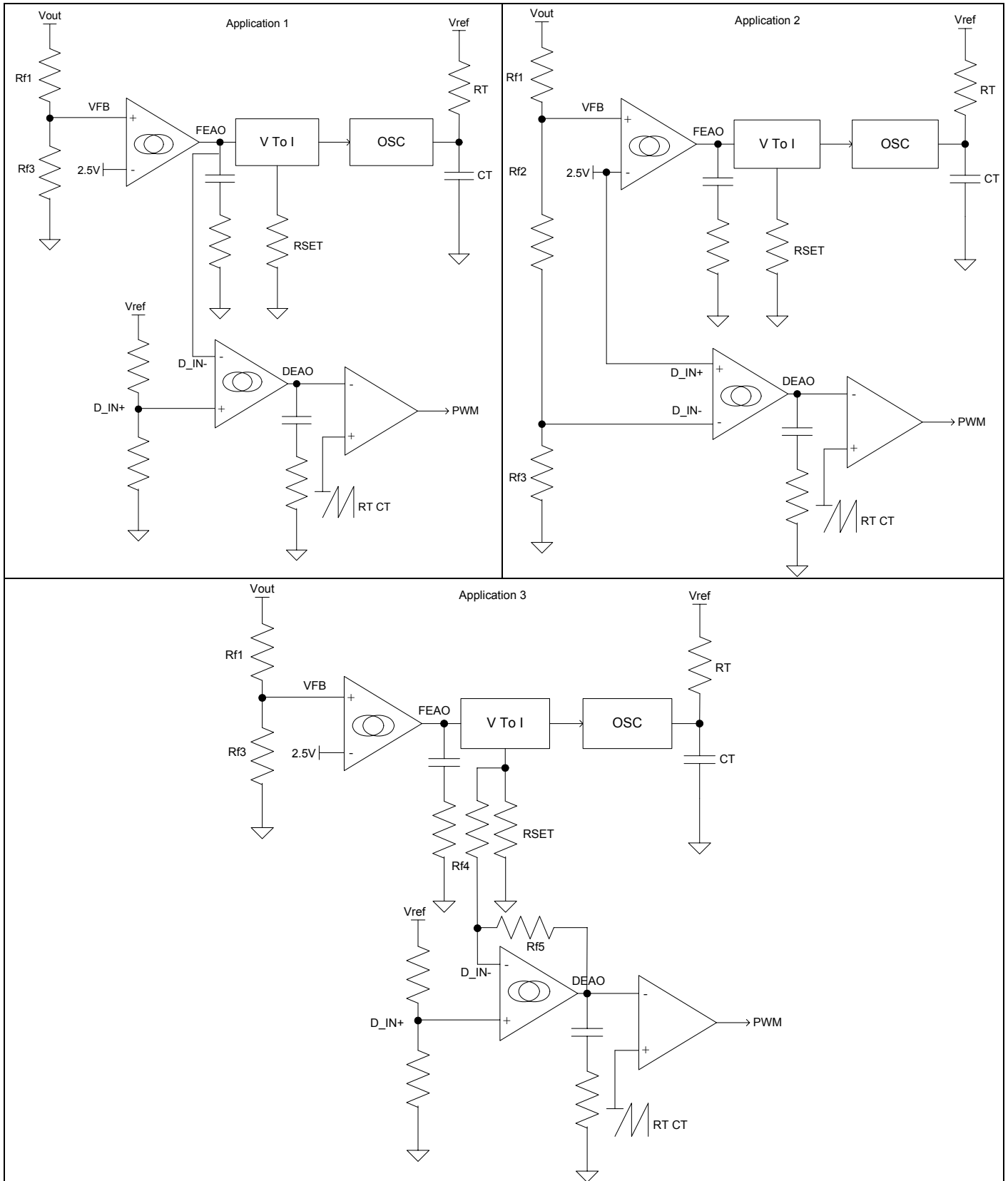
$$V_{os} = 2.5V \times R_{f2}/R_{f3}$$

When the output load is reduced to a point where FEAO is railed to its maximum value of 5V+ VBE, the frequency is fixed at a value determined by 5V+VBE. Further reduction in load will cause the controller to go into PWM mode when the voltage at the VFB pin is 2.5V+Vos. During this light load operation, FM error amplifier is in open-loop mode while PWM is in closed-loop mode. Compensation is accomplished by connecting R and C in series to the DEAO pin.

In Application 3, low gain configuration accomplished by connecting Rf4 and Rf5 in the closed loop configuration. The gain for the PWM is determined by Rf4 and Rf5 where the gain is equal to -Rf5/Rf4. The voltage of VRset at which the controller goes into FM and PWM simultaneously is equal to :

$$VR_{set} = D_IN+ \times (1+R_{f4}/R_{f5}) - (R_{f4}/R_{f5}) \times 3 \text{ where } 3 \text{ is the peak voltage of } RTCT$$

Varyin Rset from VRset to VRset + 1.75 × Rf4/Rf5 will cause the duty cycle to vary from 50% to 0% while the frequency will vary proportionally according to 1.75*Rf4/Rf5 where 1.75 is the peak-to-peak voltage of the RTCT ramp. For proper operation, select Rf5 value so that the current through Rf5 {(D_IN+) - 1.2}/Rf5 should be less than 5uA.

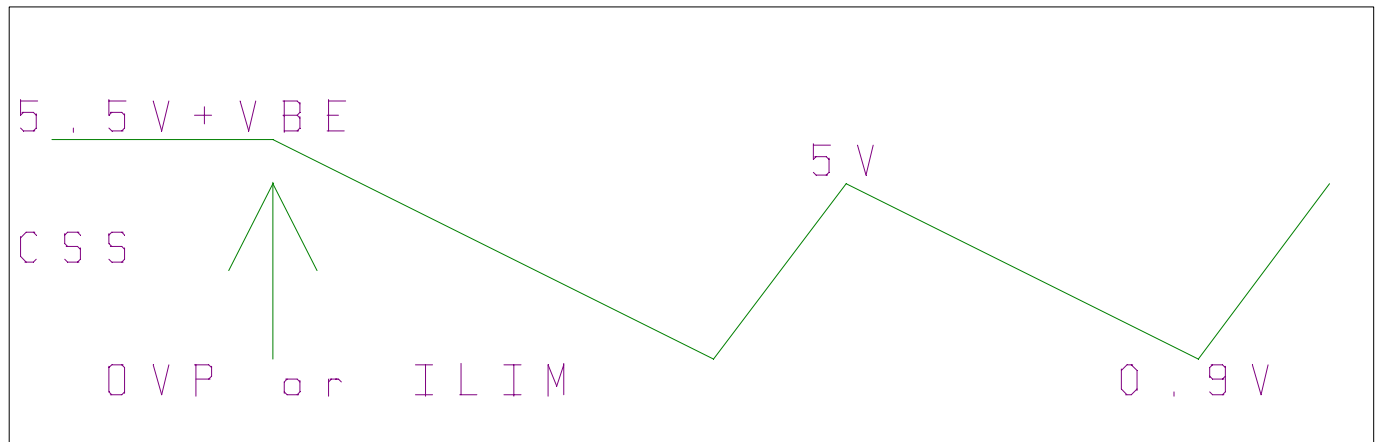


Soft Start and Enable

Soft start of the FM and PWM is controlled by the selection of the external capacitor at CSS pin. A current source of 8uA supplies the charging current for the capacitor. Soft start of the FM and PWM begins at 1.25V. The soft start pin CSS also serves as an enable function. The output drivers are enabled when CSS pin reached 1V.

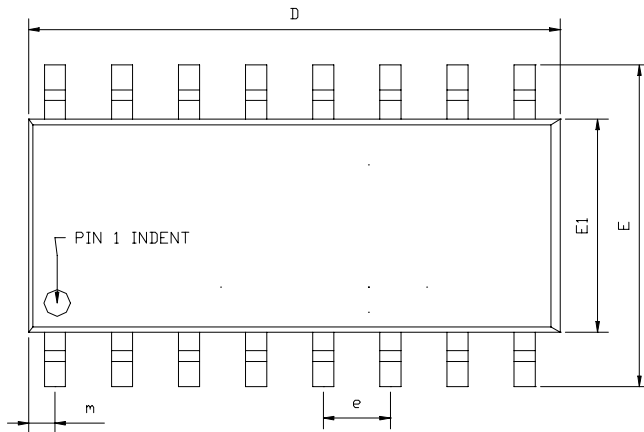
Auto-retry Mode

During normal operation, CSS pin will be charged to $5.5V + V_{BE}$. When VFB exceeds 2.93V due to OVP or ILIM exceeds 1V due to over current condition, output drivers are immediate set to low, and CSS begins to discharge with 3.3uA current source. When CSS pin is below 0.9V, 8uA current source start charging the CSS pin. When CSS pin reaches 1V, the output drivers are re-enable and the controller goes into soft start mode. If OVP or over current condition still exists then, the outputs are immediately disabled, but CSS continues to charge toward 5V. When CSS reaches 5V, 8uA charging current is disabled and 3.3uA current source begins to discharge the CSS, and the cycle repeat until OVP or over current condition is removed.



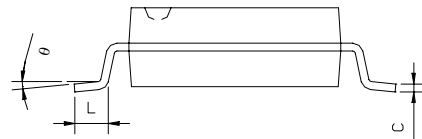
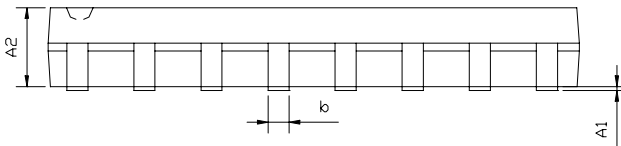
PACKAGE DIMENSION

16-PIN PSOP (PS16)



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX	MIN	NOM	MAX
A1	0.05	---	0.15	0.002	---	0.006
A2	1.40	---	1.55	0.055	---	0.061
b	0.30	---	0.51	0.012	---	0.020
C	0.15	---	0.26	0.006	---	0.010
D	9.80	---	10.06	0.386	---	0.396
E	5.79	---	6.20	0.228	---	0.244
E1	3.76	---	4.01	0.148	---	0.158
e	---	1.27	---	---	0.050	---
L	0.38	---	0.69	0.015	---	0.035
m	0.43	---	0.69	0.017	---	0.027
θ	0°	---	8°	0°	---	8°

EXPOSED PAD DIMENSION : (mm)
 PAD SIZE: X=2.3 ; Y=2.8



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